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09/380,994	09/13/1999	MASARU TAKADA	P23128USA	3373

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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/380,994	TAKADA ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,10,15 and 18-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,10,15 and 18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 claims an equal number of conductive layers on opposite sides of a central insulating layer. However, since claim 1, from which claim 19 depends establishes an odd number of conductive layers, there cannot be an equal number of conductive layers on opposite sides of a central insulating layer. For evaluation under art, the Examiner deems claim 19 as not further limiting claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,744,758 (Takenouchi).

Takenouchi discloses, referring to figure 3, a printed wiring board (10) comprising an odd number n (n=3) of conductive layers (22) which are built up via a same odd number of insulating layers (14) respectively and are electrically connected to one another via through holes (18); wherein the first conductive layer is a layer on which an electronic component is to be mounted and which conducts electric currents in and out of the electronic component (col. 6, lines 40-45), an n-th conductive layer is an external connecting layer for connecting external connecting terminals (24) which conduct electric currents in and out of the printed wiring board; a second to (n-1)-th conductive layers are current transmitting layers for transmitting internal currents of the printed wiring board; each of said first to (n-1)-th insulating layers has at least one of the through holes with a plating film formed on a wall of the at least one through hole to connect the conductive layers; and a surface of the n-th conductive layer is covered with an n-th and outermost insulating layer with external connecting terminals being exposed, and wherein a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring board (col. 6, lines 45-55) [claims 1, 19], wherein the external connecting terminals are solder balls (24; col. 6, lines 40-45) [claim 2], wherein the central insulating layer is an (n+1)/2 - th insulating layer, and the central insulating layer has at least two through holes having the same diameter and each connected to another one of the through holes [claim 20], wherein each of the

insulating layers is selected from a group comprising epoxy resins, phenol resins, polyimide resins, polybutadiene resins, and fluororesins [claim 21].

Similarly, Takenouchi discloses, a method of manufacturing a printed wiring board having an odd number n (n=3) of conductive layers (22) which are built up with a same odd number of insulating layers (14) respectively and are electrically connected to one another by first interconnecting through holes, the method comprising the steps of: interposing the insulating layers between a second to n-th conductive layers respectively and also forming first interconnecting through holes (18) for electrically connecting the conductive layers to one another; laminating a first prepreg and a copper foil on a surface of the second conductive layer (col. 6, lines 1-5) laminating a second prepreg on a surface of the n-th conductive layer, and simultaneously press-bonding the first and second prepregs, the copper foil, the second to n-th conductive lavers and the insulating layers to form a multilayer substrate having an odd number n of insulating layers, wherein the second to n-th conductive layers are internal layers of the multilayer substrate; etching the copper foil to form a first conductive layer (col. 6, lines 10-25); forming second interconnecting through holes in a first insulating layer and forming connecting holes in an n-th insulating layer respectively; forming a metal plating film (20) for electrically connecting the first conductive layer with a second conductive layer on the walls of the second interconnecting through holes of the first insulating layer; and connecting external connecting terminals (24) to a surface of the n-th conductive layer exposed through the first connecting through holes of the n-th insulating layer [claim 3], wherein the odd number n of insulating layers includes a central insulating layer among

the second to n-th insulating layers [claim 22], wherein the odd number n of insulating layers include a central insulating layer, and the same number of the conductive layers are provided on the upper side and lower side of the central insulating layer [claim 23], wherein said forming the first interconnecting through holes includes forming at least two interconnecting through holes in a central insulating layer of the odd number of insulating layers that is connected to another one of the first interconnecting through holes or the second interconnecting through hole [claim 24], wherein each of the insulating layers is selected from a group comprising epoxy resins, phenol resins, polyimide resins, polybutadiene resins, and fluororesins (col. 5, line 65 – col. 6, line 5) [claim 25].

Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6,132,853 (Noddin).

Noddin discloses, referring primarily to figure 1, a printed wiring board comprises an internal insulating substrate (4) having a conductor circuit (6) formed on a surface thereof, an internal insulating layer (3,7) laminated on the surface of the internal insulating substrate, and an external insulating layer (8) laminated on a surface of the internal insulating layer, the internal insulating layer and the external insulating layer having an internal conductor circuit (5) and an external conductor circuit (10) respectively; wherein the internal insulating layer comprising two or more internal insulating layers (3, 7) of glass cloth-reinforced prepreg containing 30 to 70 % by weight of glass cloth (col. 27, lines 15-35) and wherein the external insulatinq laver comprises

synthetic resins and inorganic fillers or synthetic resin single substances (col. 27, lines 15-35) [claim 4].

Claims 7, 10, 15, and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,764,485 (Lebaschi).

Lebaschi discloses, referring primarily to figures 6-7, a method of manufacturing a printed wiring board having a plurality of conductive layers which are built up via insulating layers respectively and are electrically connected to one another by interconnecting through holes (30), the method comprising the steps of: forming conductive layers on a plurality of insulating layers respectively (20-26), wherein each of the insulating layers is selected from a group comprising resin base materials containing a single synthetic resin substance, resin base materials containing synthetic resins and inorganic fillers, and cloth base materials containing synthetic resins and inorganic cloth (col. 2, lines 45-55); laminating and press-bonding the resulting insulating layers to form a multilayer substrate; irradiating a laser beam on the multilayer substrate at interconnecting through hole-forming portions to define interconnecting through holes with bottoms defined by the conductive layers (col. 2, lines 45-50) covering the walls of the interconnecting through holes with metal plating films (28); and fusing solder balls (13) against the interconnecting through holes and filling them with solder (15) [claim 7], wherein the insulating layers are flexible films made of a glass fiber-reinforced resin (col. 2, lines 45-50) [claim 10], wherein the inorganic fillers are selected from a group comprising glass short fibers, silica, mica, alumina, and carbon (col. 2, lines 45-50)

[claim 26], wherein the cloth base materials are selected from a group comprising glass-fiber cloth, carbon cloth, and aramid cloth (col. 2, lines 45-50) [claim 27].

Similarly, Lebaschi discloses, referring primarily to figures 1 and 7, a printed wiring board comprising: an insulating substrate (21-24) having at least one interconnecting through hole (18) penetrating the insulating substrate; an annular pad (17) disposed along a peripheral edge of a first opening of the interconnecting through hole so as not to cover the first opening, a covering pad (34) covering a second opening of the interconnecting through hole; a conductor circuit connected to the covering pad; a metal plating film (28) electrically connecting the annular pad and the covering pad, the metal plating film covering a wall of the interconnecting through hole and the bottom of the interconnecting through hole defined by the covering pad; and a solder ball (13) for external connection bonded on a surface of the annular pad at a position offset from the interconnecting through hole (figure 1 an col. 7, lines 10-40) [claim 15], wherein the solder ball is located in alignment with the central axis of the interconnecting through hole (figure 7) [claim 28], wherein the solder ball is located at a position offset from the interconnecting through hole (figure 1) [claim 29].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lebaschi in view of Takenouchi.

Lebaschi discloses the claimed invention as described above except Lebaschi does not specifically disclose that the surface of the insulating substrate is covered with a solder resist [claim 18]. However, Takenouchi (col. 6, lines 30-35) teaches places a solder resist on a substrate. Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to cover the substrate in the invention of

Lebaschi with a solder resist as taught by Takenouchi. The motivation for doing so would have been to prevent oxidation of the circuit patterns.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 7, 10, 15, and 18-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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